Kishankumar R. Patel

B.Tech (Electronics and Communication)

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Career Objective

To work for an organization that can provide a challenging environment to enhance the technical and professional skills.

Education

Chandubhai S. Patel Institute Of Technology (CHARUSAT University) — *Changa, Anand*

B.Tech in Electronics and Communication Engineering — *3rd year Pursuing*

- CGPA: 9.39

Dadabhai Navroji High school, GSHSEB — *Anand*

Higher Secondary education, H.S.C — *July 2014 - March 2016*

- Score : 84.33 %

Dadabhai Navroji High school, GSHSEB — *Anand*

Secondary education, S.S.C — *July 2013 - March 2014*

- Score : 85.67 %

Skills

Software Knowledge : Xilinx ISE, Icarus Verilog, ATMEL STUDIO, Arduino IDE, Proteous, 8086 Emulator
Hardware Knowledge : FPGA Spartan 6, 8086 microprocessor, AVR microcontroller, LPC2148, Arduino
Languages : Verilog HDL, C, Python, C++
Communication Protocol : USART, SPI, I2C
Subject Interest : Digital Circuits, Digital System Design Using Verilog, VLSI, 8086 Microprocessor, AVR Micro-controller

Projects

Implementation of RTL code for generalized 8-bit Sequence Detector(256 sequences) — *CHARUSAT, Changa*

Responsibilities — *Feb, 2019*

- Developed RTL code for each state with functionality of changing the sequence on reset.
- Verified this RTL code by testbench.

Technologies

Language : Verilog HDL

Software : Xilinx ISE

Available on : `https://github.com/kishanpatelec/Overlapping-8-bit-Sequence-detector-for-256-sequences`

Implementation of RTL code of UART for Bluetooth module — *CHARUSAT, Changa*

Responsibilities — *Jan, 2019*

- Developed RTL code for Baud Rate Generator, Rx and Tx.
- Implemented on Hardware: Bluetooth module to mobile and mobile to bluetooth module communication.

Technologies

Language : Verilog HDL

Hardware : Waxwing SPARTAN 6 FPGA Development Board, Bluetooth module HC-05

Tool : Mobile App Bluetooth Terminal

Available on : `https://github.com/kishanpatelec/UART-for-bluetooth-module`

Distance measurement with FPGA using Ultrasonic Sensor — *CHARUSAT, Changa*

Responsibilities — *Oct, 2018*

- Developed RTL code for calculating distance.
- Developed RTL code to display the distance on 3 digit seven-segments.

Technologies

Language : Verilog HDL

Hardware : Waxwing SPARTAN 6 FPGA Development board, Ultrasonic sensor HC-SR04

Available on : `https://github.com/kishanpatelec/Distance-measurement`

Design and Development of multi floor Elevator System using micro controller *CHARUSAT, Changa*

RESPONSIBILITIES *Oct, 2018*

- Developed Embedded C code for 8 floor Elevator System.
- Developed working model in Proteus.

Technologies

Language : Embedded C

Software : Atmel Studio 7, Proteus

Summer Internship

Scripting languages: Perl & TCL *eInfochips, Ahmedabad*

RESPONSIBILITIES *24 May - 5 July 2019*

- Exercises on Perl & TCL
- Presentations : ASIC Flow, Wireless charging technology

Robot Operating System(ROS) *CHARUSAT, Changa*

RESPONSIBILITIES *14 May -2 June 2018*

- ROS File System, ROS Packages, ROS Graph Layer
- Basics of OpenCV
- Designed robot model through packages, XML file and launch file

Extracurricular Activity

Techfest : Cognizance(Chandubhai S. Patel Institute of Technology, CHARUSAT) *Changa, Anand*

GAINED KNOWLEDGE AND LEARNED BY ACTIVELY PARTICIPATING IN TECHFEST *20-21 Sep. 2018*

- Participated in event Line Ranger
- Made an automated robot called line follower robot
- Secured 3rd position

Techfest : Footprints(Maharaja Sayajirao University) *Vadodara, Gujarat*

GAINED KNOWLEDGE AND LEARNED BY ACTIVELY PARTICIPATING IN TECHFEST *23-24 Feb. 2018*

- Participated in group event ROBOWAR(fight of robots)
- Made a mechanical robot with enhanced design and structure
- Secured 5th position among 24 groups from all over India

Techfest : Tesseract(Pandit Deendayal Petroleum University) *Gandhinagar, Gujarat*

GAINED KNOWLEDGE AND LEARNED BY ACTIVELY PARTICIPATING IN TECHFEST *11 Nov. 2017*

- Participated in group event ROBOWAR(fight of robots)
- Made a mechanical robot
- Secured first position

References

Prof. Jignesh Patoliya
CHARUSAT, Changa
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Prof. Dharmendra Chauhan
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Declaration

I hereby declare that the information furnished above is true to the best of my knowledge. I do hereby declare that above particulars of information and facts stated are true, correct and complete to the best of my knowledge and belief.

Place : Anand

Signature

Date : 15/03/2019

Kishankumar R. Patel